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February 12, 2002

To: Commissioner of Patents and Trademarks $/\!\!/$ 

Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572

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Subject:

Serial No. 10/002,987 11/30/09

Feng Dai, Pang Choong Hau, Peter Hing, Lap Chan

A NOVEL METHOD TO ACHIEVE STI PLANARIZATION

Grp. Art Unit:

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February ), 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

2/15/0

CS-00-197/199

Co-pending U.S. Patent Application Serial No. 09/439,357 (CS-99-059), filed on Nov. 15 1999, now issued as U.S. Patent 6,197,691 to Lee, "Shallow Trench Isolation Process," teaches a new technique for preventing dishing in an STI process.

Co-pending U.S. Patent Application Serial No. 09/803,187 (CS-00-138) to V.L.S. Keong et al., filed on March 12, 2001, is an improvement over U.S. Patent 6,197,691 where the HF dip step is not required.

- U.S. Patent 6,057,210 to Yang et al., "Method of Making a Shallow Trench Isolation for ULSI Formation Via In-Direct CMP Process," discloses a process in which corners of the silicon nitride areas are exposed using a wet etch.
- U.S. Patent 6,015,755 to Chen et al., "Method of Fabricating a Trench Isolation Structure Using a Reverse Mask," discloses a partial reverse mask process in which a reverse mask is formed over wide areas.

The following two U.S. Patents teach reverse mask processes:

- 1) U.S. Patent 4,954,459 to Avanzino et al., "Method of Planarization of Topologies in Integrated Circuit Structures."
- 2) U.S. Patent 5,961,794 to Morita, "Method of Manufacturing Semiconductor Devices."

The following three U.S. Patents teach CMP processes:

- 1) U.S. Patent 5,923,993 to Sahota, "Method for Fabricating Dishing Free Shallow Isolation Trenches."
- 2) U.S. Patent 6,057,207 to Lin et al., "Shallow Trench Isolation Process Using Chemical-Mechanical Polish with Self-Aligned Nitride Mask on HDP-Oxide."
- 3) U.S. Patent 6,103,581 to Lin et al., "Method for Producing Shallow Trench Isolation Structure."
- U.S. Patent 6,004,863 to Jang, "Non-Polishing Sacrificial Layer Etchback Planarizing Method for Forming a Planarized Aperture Fill Layer," discloses isotropic etching of oxide peaks.

Sincerely,

Stephen B. Ackerman, Reg. No. 37761